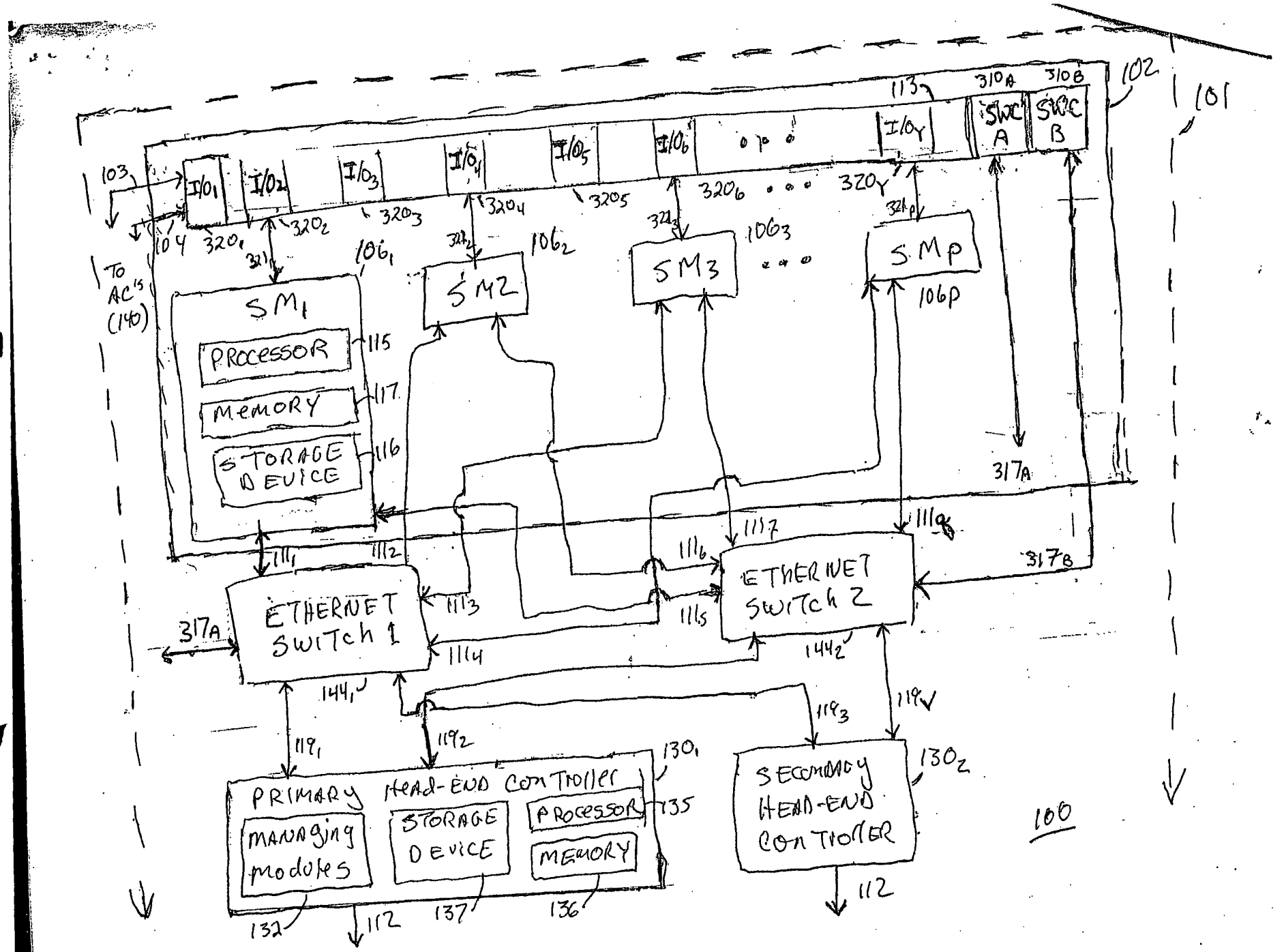
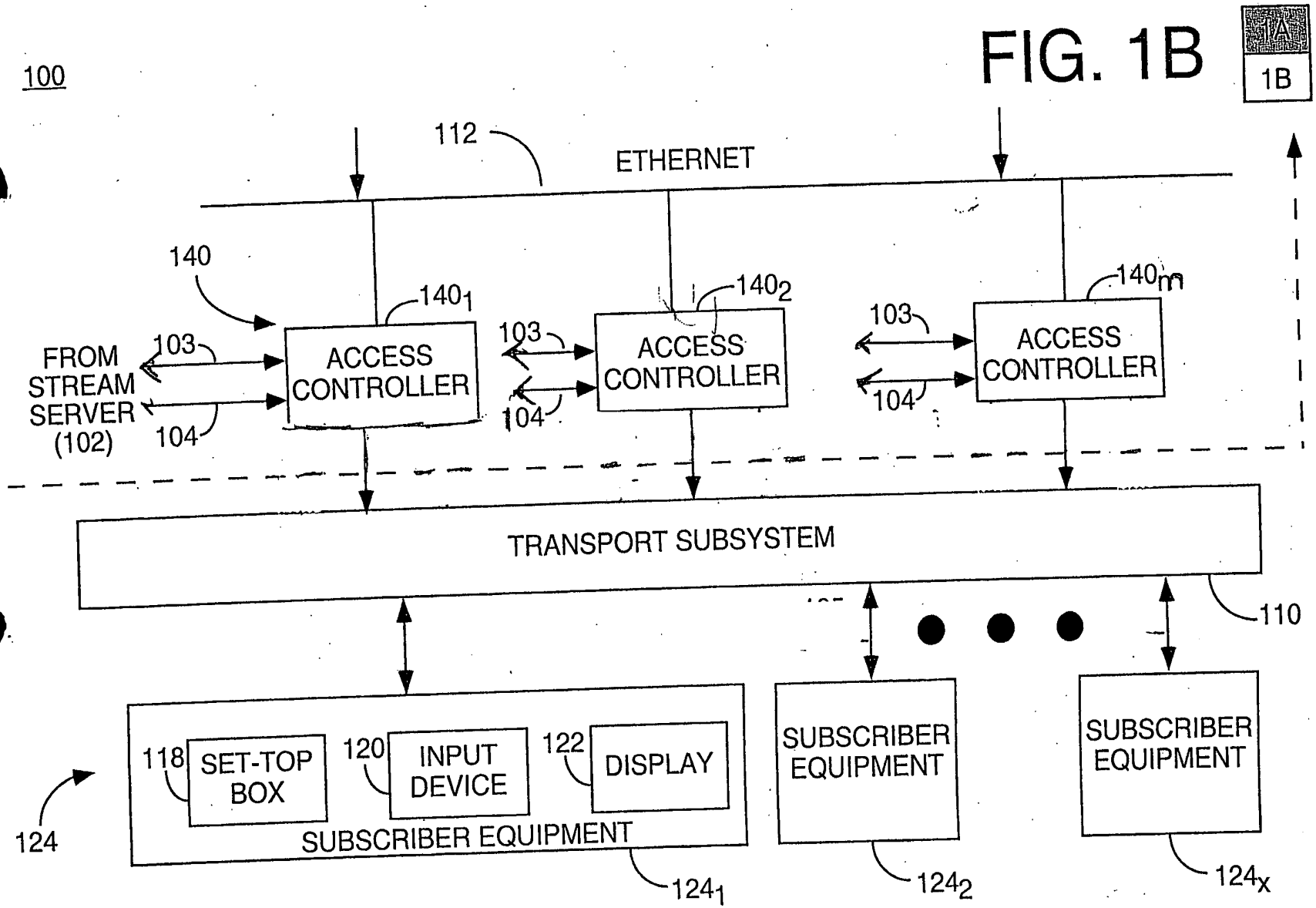
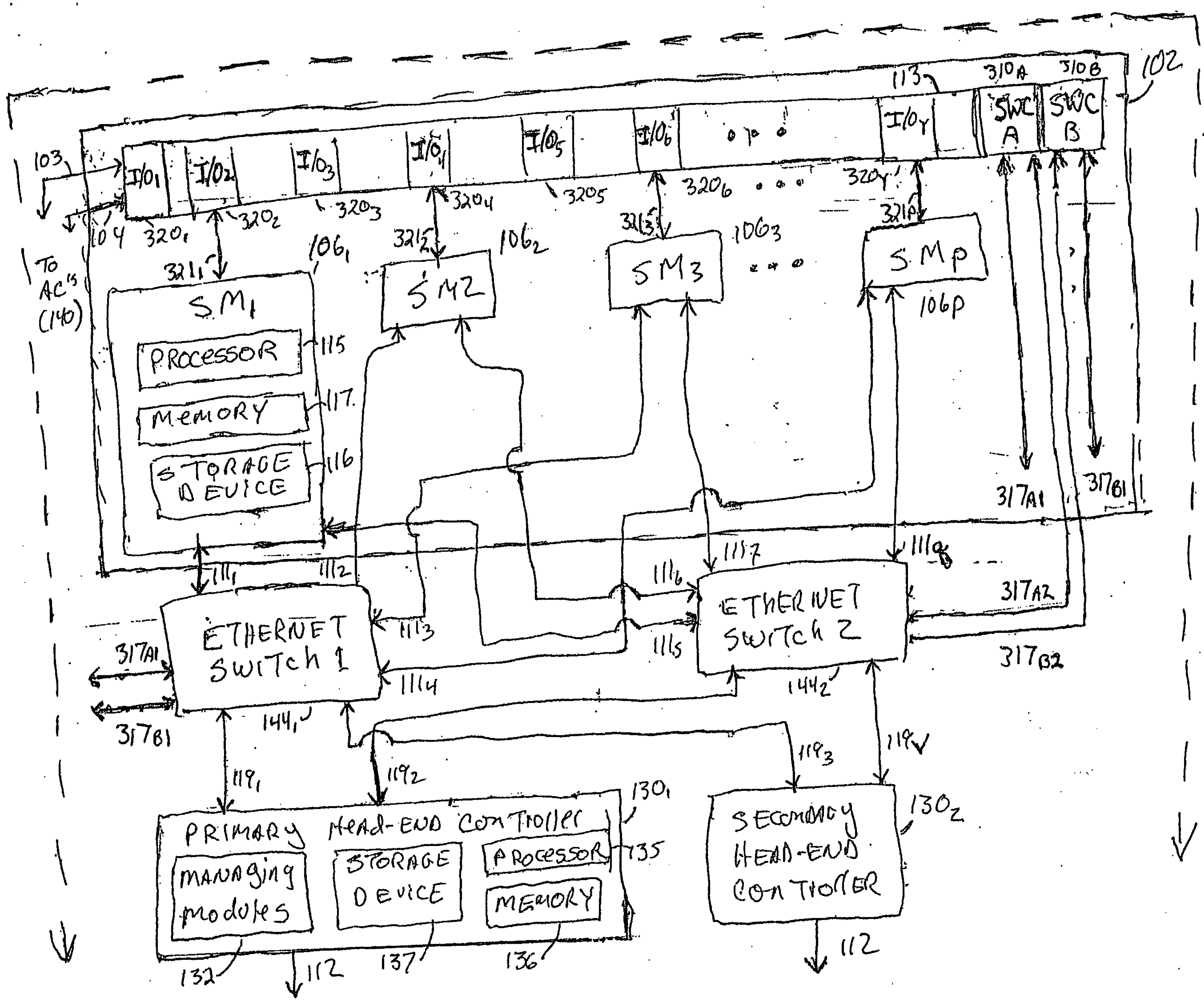

102
101
113
310A
310B
103
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/OY
SWC A
SWC B
104
320Y
321
321p
322p
To AC's (140)
SM1
SM2
SM3
SMp
PROCESSOR
MEMORY
STORAGE DEVICE
115
117
116
106p
317A
317B
111
112
113
114
115
116
117
ETHERNET SWITCH 1
ETHERNET SWITCH 2
144
119
PRIMARY HEAD-END CONTROLLER
MANAGING modules
STORAGE DEVICE
PROCESSOR
MEMORY
SECONDARY HEAD-END CONTROLLER
130
135
132
137
136
100

FIG. 1A

FIG. 1B

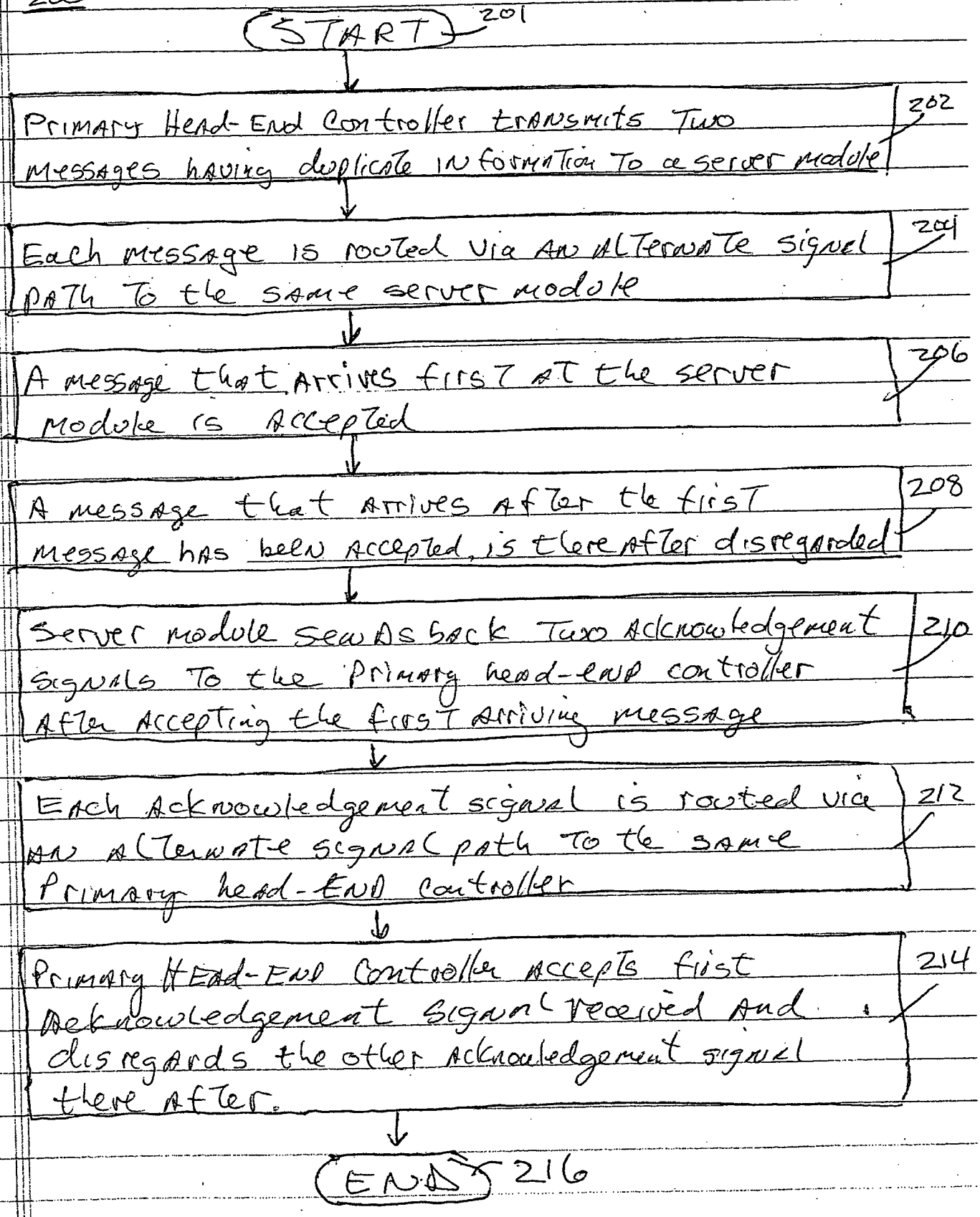

100
112
ETHERNET
140
140_1
140_2
140_m
FROM STREAM SERVER (102)
103
104
ACCESS CONTROLLER
ACCESS CONTROLLER
ACCESS CONTROLLER
TRANSPORT SUBSYSTEM
110
118
SET-TOP BOX
120
INPUT DEVICE
122
DISPLAY
SUBSCRIBER EQUIPMENT
124
124_1
SUBSCRIBER EQUIPMENT
124_2
SUBSCRIBER EQUIPMENT
124_x
1A
1B



0051017 9.033100

FIG. 1C

FIG. 2


200
START
201
Primary Head-End Controller transmits Two Messages having duplicate information To a server module
202
Each message is routed via An Alternate signal path To the same server module
204
A message that Arrives first At the server module is Accepted
206
A message that Arrives After the first message has been Accepted, is there after disregarded
208
Server module sends back Two Acknowledgement Signals To the Primary head-end controller After Accepting the first Arriving message
210
Each Acknowledgement signal is routed via An Alternate signal path To the same Primary head-End controller
212
Primary Head-End Controller accepts first Acknowledgement Signal received And disregards the other Acknowledgement signal there After.
214
END
216

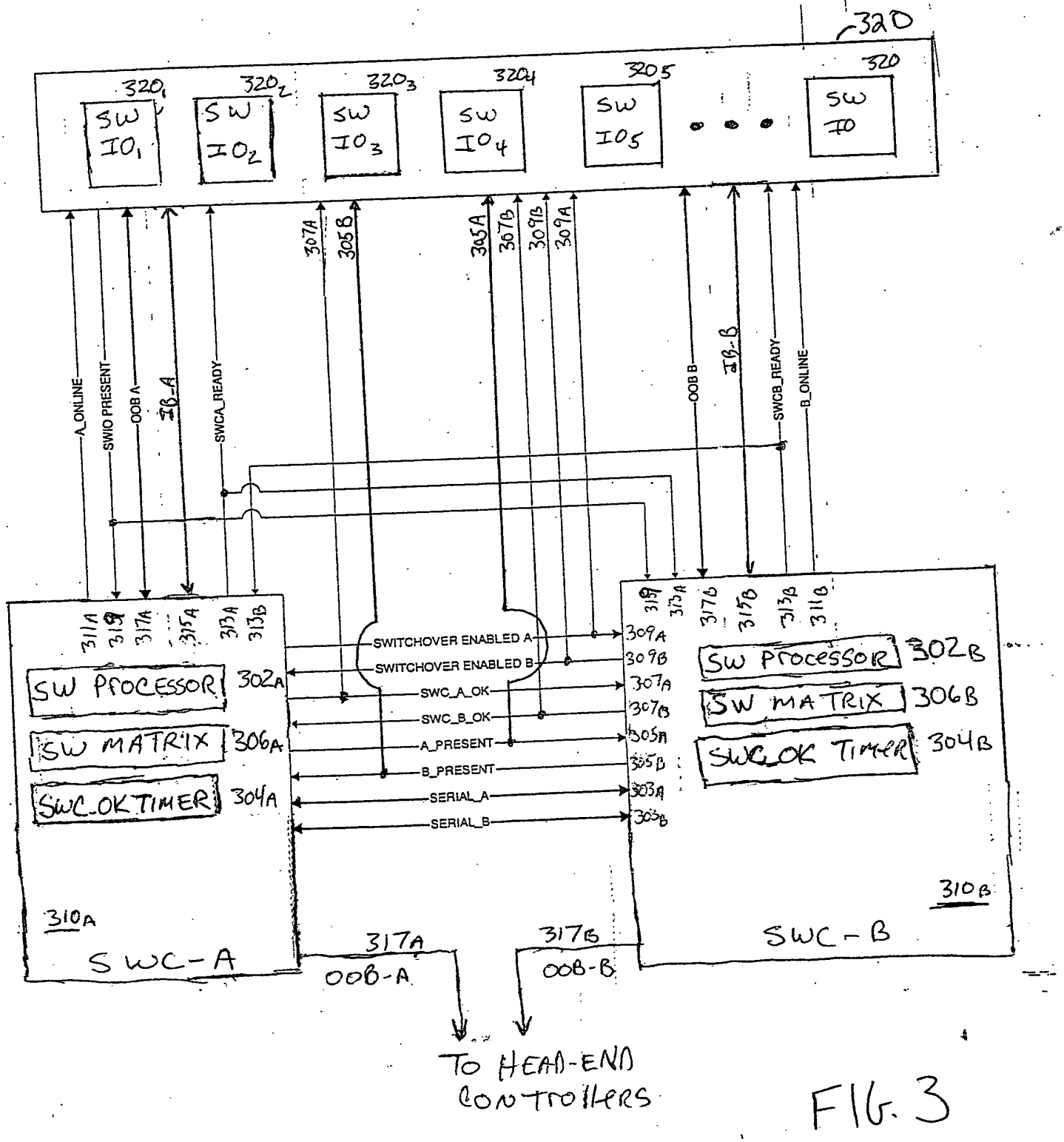
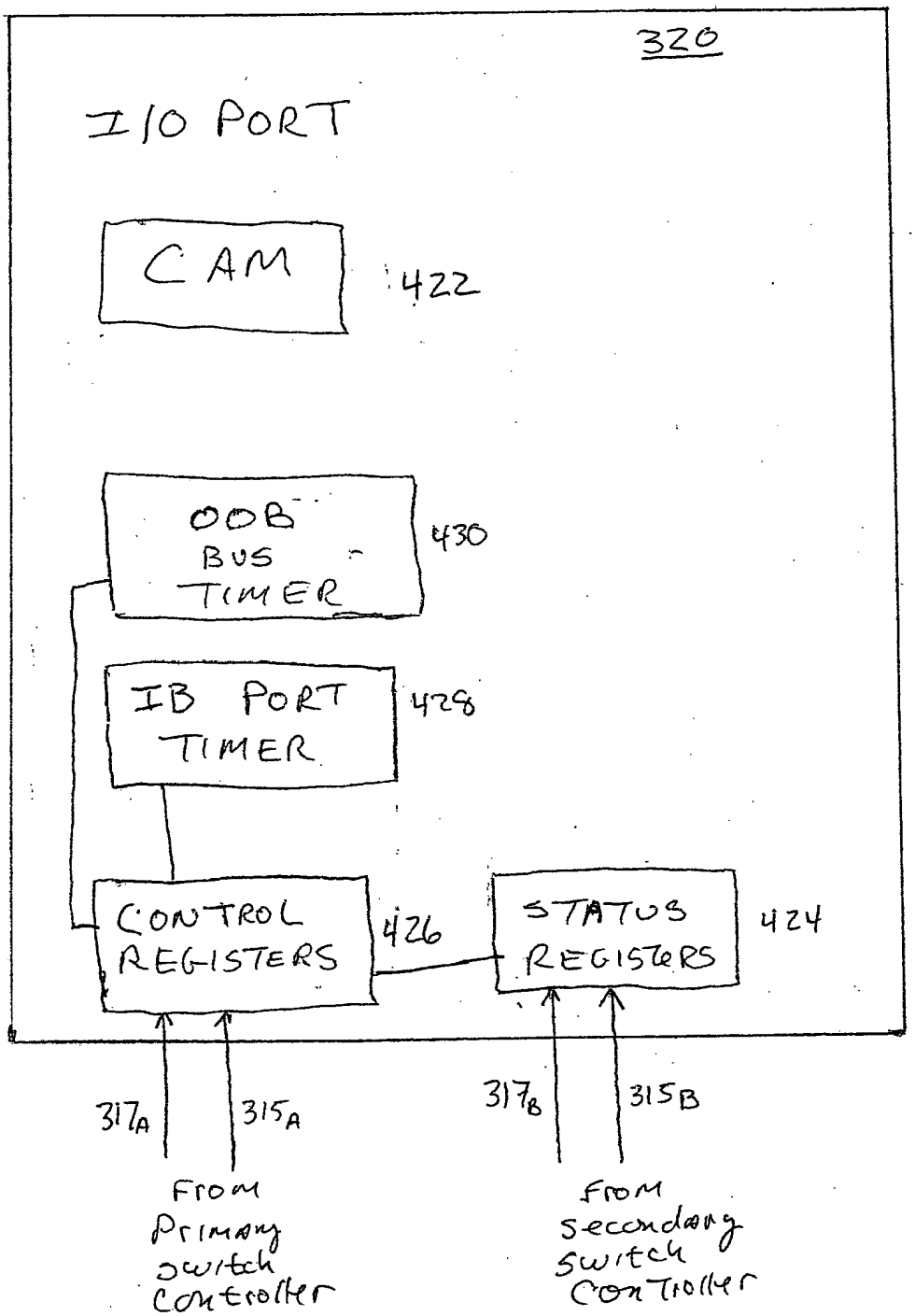

320
320₁
SW IO₁
320₂
SW IO₂
320₃
SW IO₃
320₄
SW IO₄
320₅
SW IO₅
320
SW IO
A_ONLINE
SWIO PRESENT
OOB A
IB-A
SWCA_READY
307A
305B
305A
307B
309B
309A
OOB B
IB-B
SWCB_READY
B_ONLINE
311A
319
317A
315A
313A
313B
SW PROCESSOR 302A
SW MATRIX 306A
SWC_OK TIMER 304A
SWITCHOVER ENABLED A
SWITCHOVER ENABLED B
SWC_A_OK
SWC_B_OK
A_PRESENT
B_PRESENT
SERIAL_A
SERIAL_B
309A
309B
307A
307B
305A
305B
303A
303B
319
317A
317B
315B
313B
311B
SW PROCESSOR 302B
SW MATRIX 306B
SWC_OK TIMER 304B
310A
SWC-A
310B
SWC-B
317A
OOB-A
317B
OOB-B
TO HEAD-END CONTROLLERS

FIG. 3

FIG. 4


320
I/O PORT
CAM
422
OOB BUS TIMER
430
IB PORT TIMER
428
CONTROL REGISTERS
426
STATUS REGISTERS
424
317A
315A
317B
315B
From Primary switch Controller
From secondary switch Controller

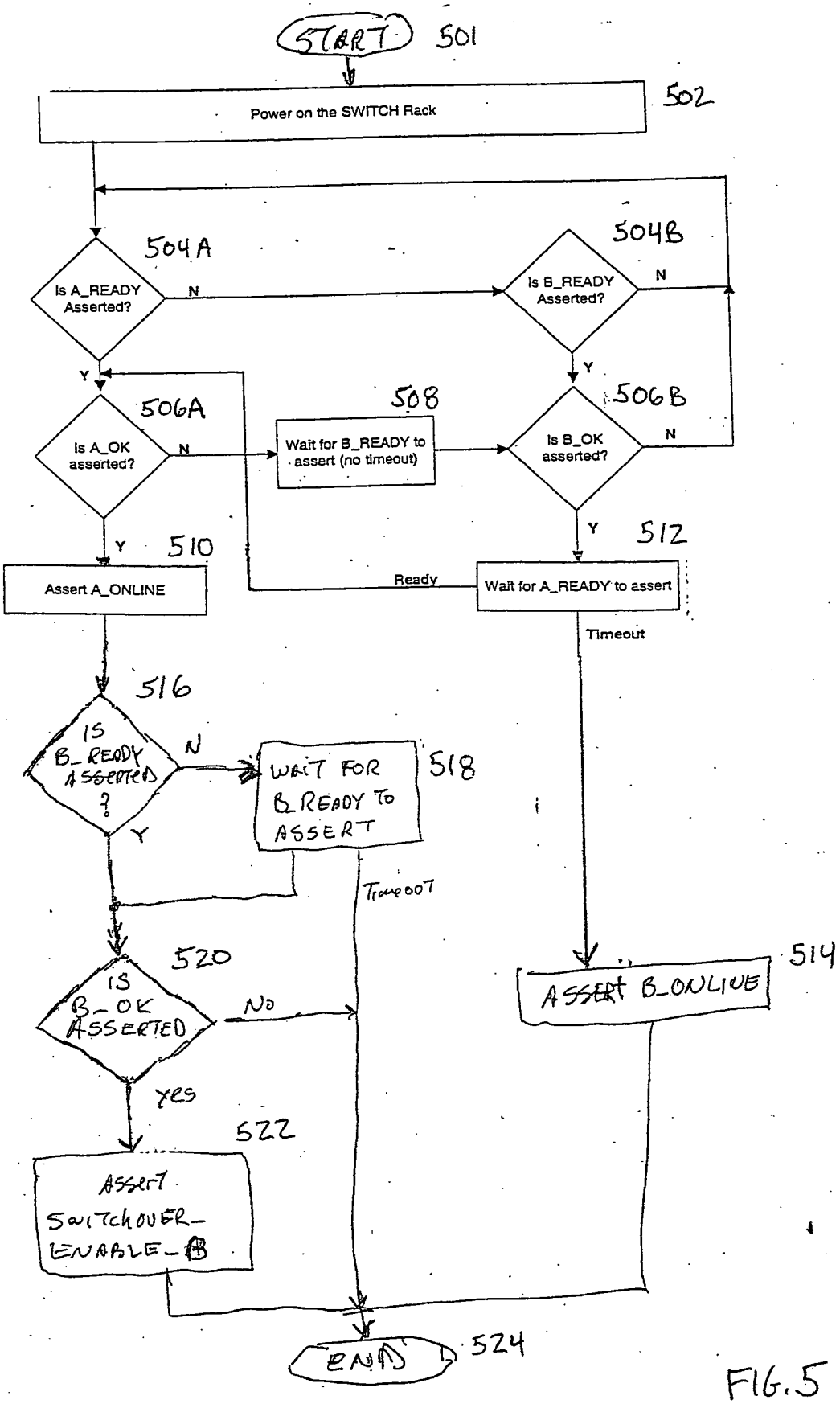

START
501
Power on the SWITCH Rack
502
504A
Is A_READY Asserted?
N
504B
Is B_READY Asserted?
N
Y
Y
506A
Is A_OK asserted?
N
508
Wait for B_READY to assert (no timeout)
506B
Is B_OK asserted?
N
Y
Y
510
Assert A_ONLINE
Ready
512
Wait for A_READY to assert
Timeout
516
IS B_READY ASSERTED ?
N
Y
518
WAIT FOR B_READY TO ASSERT
Timeout
520
IS B_OK ASSERTED
No
yes
514
ASSERT B_ONLINE
522
ASSERT SWITCHOVER_ENABLE_B
524
END

FIG. 5

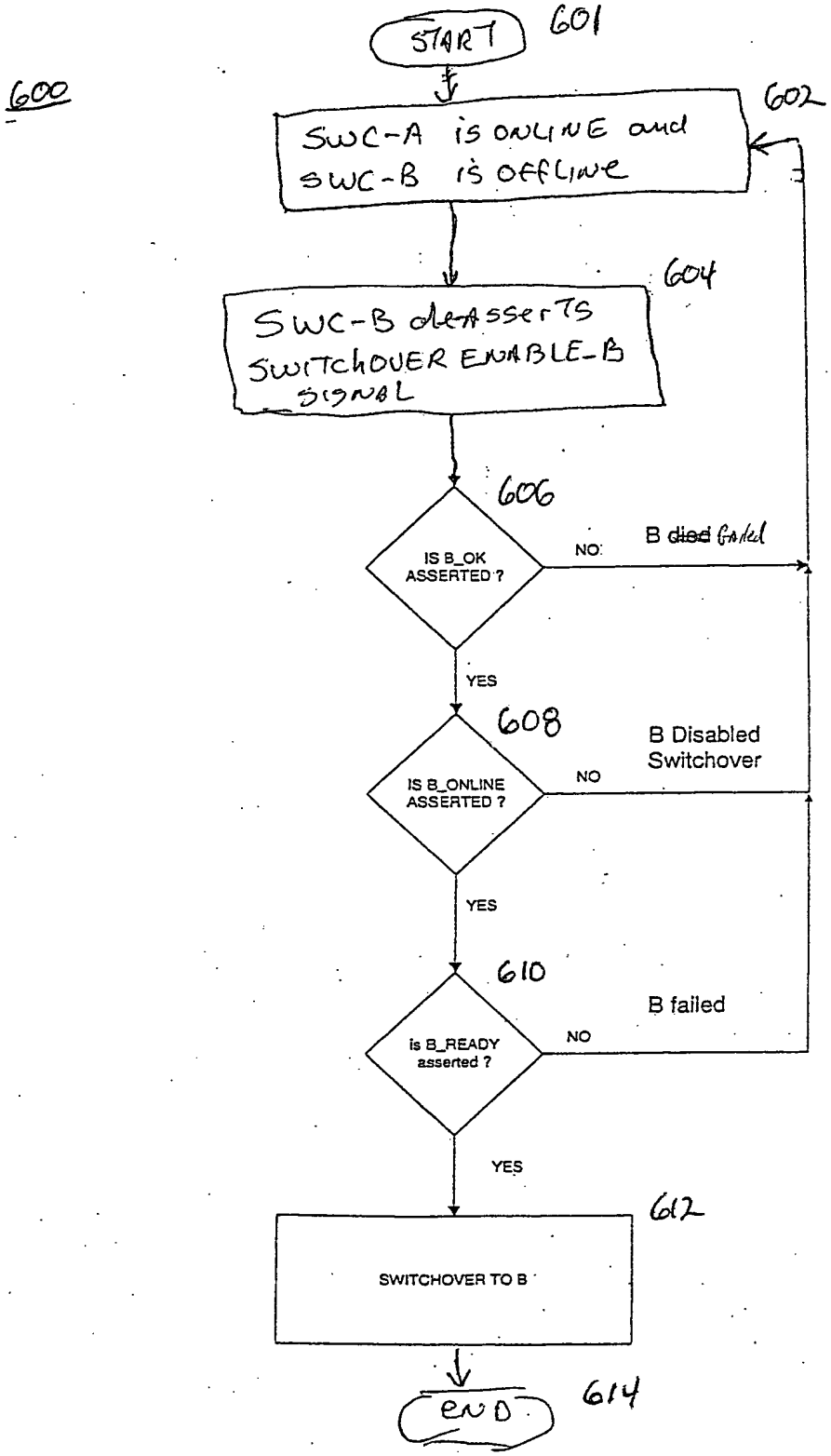

600
START
601
SWC-A is ONLINE and SWC-B is OFFLINE
602
SWC-B deasserts SWITCHOVER ENABLE-B signal
604
IS B_OK ASSERTED ?
606
NO
B ~~died~~ failed
YES
IS B_ONLINE ASSERTED ?
608
B Disabled Switchover
NO
YES
is B_READY asserted ?
610
B failed
NO
YES
SWITCHOVER TO B
612
END
614

FIG. 6.

Fig. 7

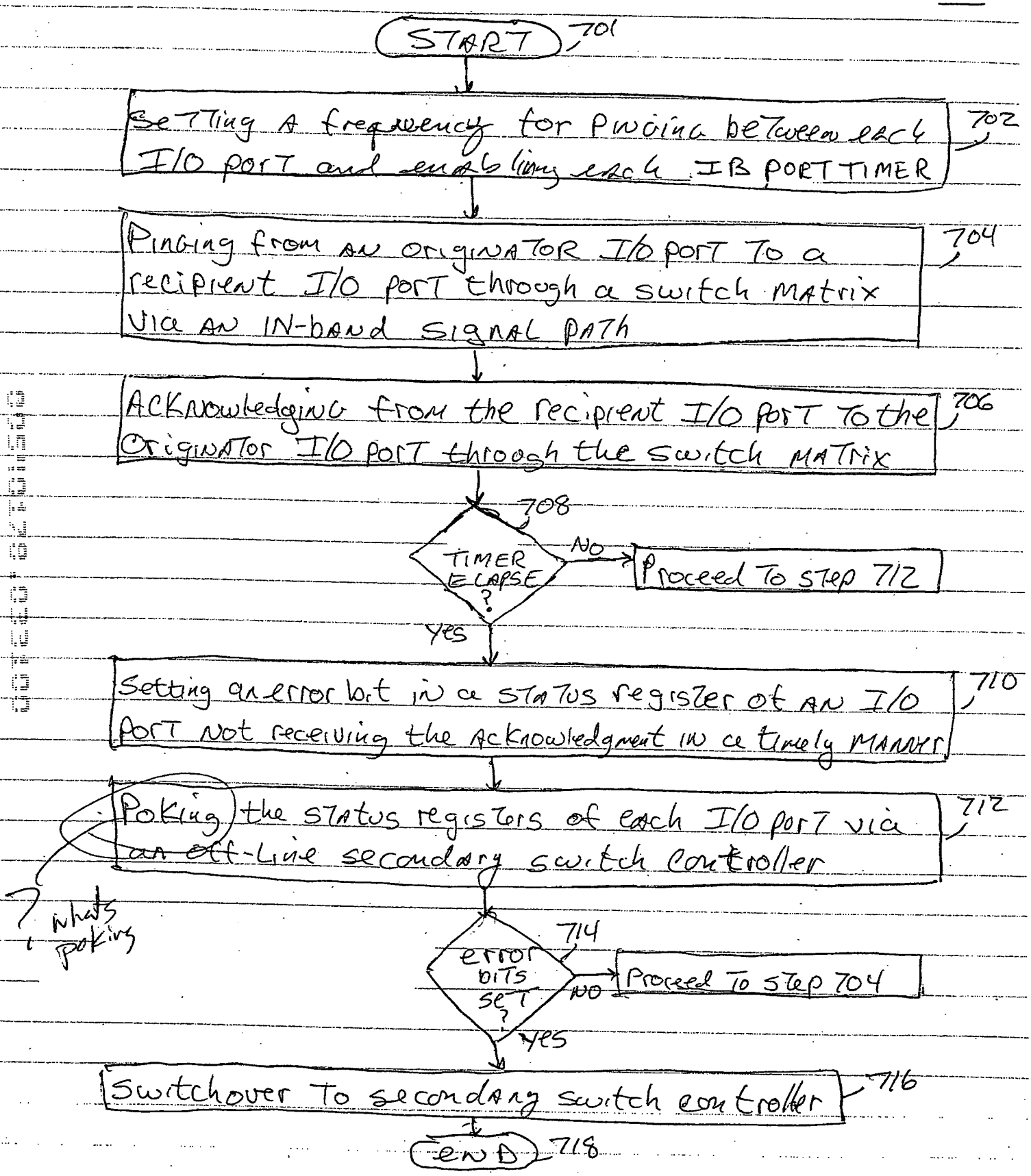
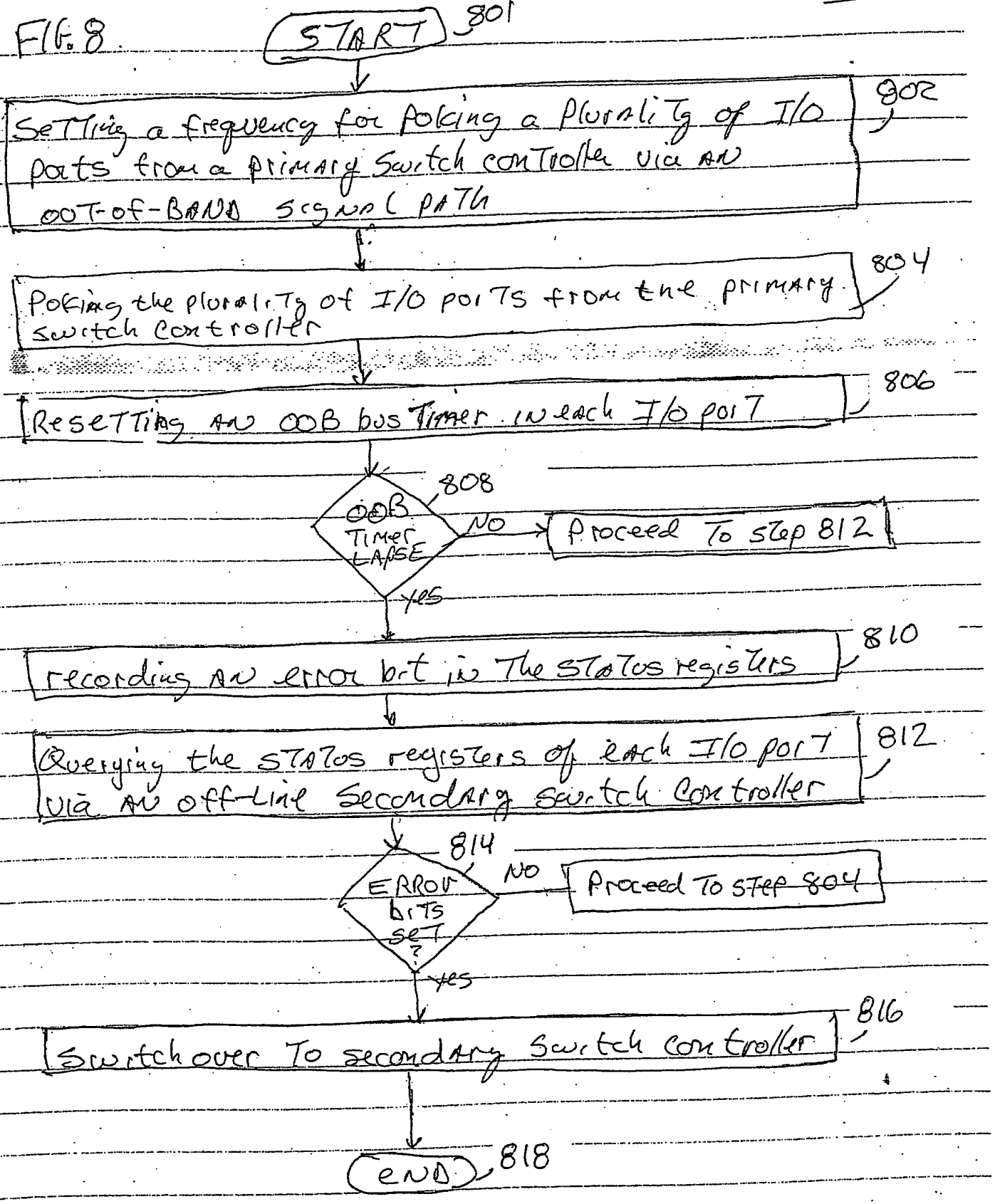

700
START
701
Setting A frequency for pinging between each I/O port and enabling each IB PORT TIMER
702
Pinging from an originator I/O port To a recipient I/O port through a switch MATRIX via AN IN-band SIGNAL PATH
704
ACKnowledging from the recipient I/O port To the originator I/O port through the switch MATRIX
706
708
TIMER ELAPSE ?
No
Proceed To step 712
Yes
Setting an error bit in a STATUS register of AN I/O port Not receiving the Acknowledgment in a timely MANNER
710
Poking the STATUS registers of each I/O port via an off-Line secondary switch controller
712
whats poking
714
error bits set ?
no
Proceed To step 704
yes
Switchover To secondary switch controller
716
END
718

FIG. 8


800
START
801
Setting a frequency for poking a plurality of I/O ports from a primary switch controller via an out-of-band signal path
802
Poking the plurality of I/O ports from the primary switch controller
804
Resetting an OOB bus Timer in each I/O port
806
OOB Timer Lapse
808
NO
Proceed To step 812
yes
recording an error bit in the status registers
810
Querying the status registers of each I/O port via an off-line secondary switch controller
812
Error bits set ?
814
NO
Proceed To step 804
yes
Switchover To secondary switch controller
816
END
818